IN THE CLAIMS

1. (Currently amended) A nonvolatile memory comprising:

a plurality of pages storing data;

a page buffer temporarily storing data by the page;

a correction circuit for correct a bit error of source data of a specific one of the pages;

a transferring circuit configured to provide the source data to the correction circuit from the page buffer and to provide amended data to the page buffer from the correction circuit after the correction circuit has corrected the bit error; and

a replicating circuit configured to copy the source data into the page buffer and to store the amended data into another page from the page buffer.

2. (Original) The nonvolatile memory of claim 1, wherein the source data contains old parities.

3. (Original) The nonvolatile memory of claim 2, wherein the correction circuit generates new parities from the source data, and compares the new parities with the old parities.

4. (Currently amended) The nonvolatile memory of claim 3, wherein:

the correction circuit comprises a circuit for generating column parities for bits composing one byte of the source data; and a circuit for generating line parities for bytes of the source data; and

for a one bit error in the source data, the line parities indicate a binary weighted line address and its complement of the one bit error in the page buffer, and the column parities indicate a binary weighted column address and its complement of the one bit error in the page buffer.

5. (Original) The nonvolatile memory of claim 1, wherein the nonvolatile memory is a NAND flash memory.

6. (Currently amended) A nonvolatile memory comprising:

a data field composed of a plurality of pages for storing data;

a first storage configured to store first parities in a predetermined region of the data field, the first parities being generated during a programming operation for the page;

a page buffer for temporarily storing data by the page;

a moving circuit configured to copy source data stored in a ~~specific~~ first one of the pages into the page buffer;

a parity circuit configured to generate second parities from the source data stored in the page buffer;

a correction circuit configured to generate modified data from the source data in response to a result of comparing the first parities with the second parities; and

a transfer circuit configured to transfer the modified data of the source data to the page buffer ~~in response to a result of comparing the first parities with the second parities;~~

wherein the moving circuit is further configured to copy the modified data in the page buffer to a second one of the pages after the correction circuit has generated the modified data.

7. (Canceled)

8. (Original) The nonvolatile memory of claim 6, wherein the second parities comprise column parities and line parities.

9. (Original) The nonvolatile memory of claim 8, wherein the parity circuit comprises a circuit for generating column parities for bits composing one byte of the source data; and a circuit for generating line parities for bytes of the source data.

10. (Original) The nonvolatile memory of claim 6, wherein the nonvolatile memory is a NAND flash memory.

11. (Currently amended) A method of transferring source data of a ~~specific~~ first page to ~~another~~ a second page in a nonvolatile memory having a page buffer structured to temporarily store data by the page, the source data containing old parities, the method comprising:

storing the source data from the first page into the page buffer;

generating new parities from the source data stored in the page buffer;

comparing the old parities with the new parities;

creating modified data from the source data in response to a result of the comparing; and

moving the modified data to ~~the another page through~~ the page buffer after the creation of the modified data; and

storing the modified data in the page buffer in the second page.

12. (Original) The method of claim 11, further comprising storing the old parities of the source data into a predetermined field of the memory before storing the source data into the page buffer.

13. (Original) The method of claim 11, further comprising informing an error status by the comparing result of the outside of the memory.

14. (Currently amended) A nonvolatile memory comprising:

a data storage field composed of a plurality of pages storing data;

a page buffer for storing data of a ~~specific~~ first one of the pages, being connected to the data storage field; ~~and~~

an error correction circuit including: a bit error detection circuit configured to detect a bit error of the data of the specific page; and a bit error correction circuit configured to amend the bit error; ~~and~~

a transfer circuit coupled to the page buffer and the error correction circuit, and configured to transfer amended data from the error correction circuit to the page buffer after the bit error correction circuit has amended the bit error; and

a moving circuit coupled to the page buffer and the data storage field, the moving circuit configured to store the amended data in the page buffer in a second one of the pages after the transfer circuit has transferred the amended data to the page buffer.

15. (Original) The nonvolatile memory of claim 14, wherein the bit error detection circuit comprises:

a parity generator for creating new parities from the data stored in the page buffer; and

a comparator for generating error address information by comparing the new parities with old parities of the data.

16. (Original) The nonvolatile memory of claim 15, wherein the error address information is referred by the bit error correction circuit to correct the data and to transfer amended data to the page buffer.

17. (Original) The nonvolatile memory of claim 16, wherein the transfer of the amended data is managed by control signals.

18. (Currently amended) The nonvolatile memory of claim 17, wherein the moving circuit is further configured to store the amended data ~~are transcribed into the specific page and another~~ in the first page.

19. (Original) The nonvolatile memory of claim 14, wherein the nonvolatile memory is a NAND flash memory.

20. (Currently amended) The method of claim 11, wherein:

storing the source data into the page buffer further comprises storing the source data into a plurality of lines and a plurality of columns of the page buffer; and

generating new parities from the source data stored in the page buffer further comprises generating the new parities including:

a plurality of pairs of line parities, for each line parity pair, a first line parity associated with a first half of the lines, and a second line parity associated with a second half of the lines; and

a plurality of pairs of column parities, for each column parity pair, a first column parity of the pair associated with a first half of the columns, and a second column parity of the pair associated with a second half of the columns;

wherein for a one bit error in the source data, the line parities indicate a binary weighted line address and its complement of the one bit error in the page buffer, and the column

parities indicate a binary weighted column address and its complement of the one bit error in the page buffer.

21. (Previously presented) The method of claim 20, wherein generating the new parities further comprises:

for each column parity:

resetting a parity accumulator associated with the column parity; and

for each line of the page buffer:

generating a result of an exclusive-or operation on bits of the line in columns associated with the column parity; and

updating the parity accumulator with the result.

22. (Previously presented) The method of claim 21, wherein generating the new parities further comprises:

resetting a parity accumulator for each line parity; and

for each line of the page buffer:

generating a result of an exclusive-or operation on bits of the line; and

for each line parity associated with the line:

updating the parity accumulator associated with the line parity.

23. (Currently amended) A nonvolatile memory comprising:

a data storage field composed of a plurality of pages, each page configured to store data and first error correction information associated with the data;

a page buffer coupled to the data storage field, and configured to store a page of data in a plurality of lines and a plurality of columns, and configured to store the associated first error correction information;

a parity generator coupled to the page buffer, and configured to generate second error correction information from the data stored in the page buffer, the parity generator including:

a line parity circuit coupled to the page buffer and configured to generate a plurality of pairs of line parities, for each line parity pair, a first line parity associated with a first half of the lines, and a second line parity associated with a second half of the lines; and

a column parity circuit coupled to the page buffer and configured to generate a plurality of pairs of column parities, for each column parity pair, a first column parity of the pair associated with a first half of the columns, and a second column parity of the pair associated with a second half of the columns;

wherein the second error correction information includes the pairs of line parities and the pairs of column parities, and for a one bit error in the source data, the line parity pairs indicate a binary weighted line address and its complement of the one bit error in the page buffer, and the column parity pairs indicate a binary weighted column address and its complement of the one bit error in the page buffer;

a comparator coupled to the page buffer and the parity generator, and configured to compare the first error correction information to the second error correction information to generate an address information signal; and

an error correction logic circuit coupled to the page buffer and the comparator, and configured to generate amended data and control signals in response to the address information signal and the data;

wherein the page buffer is configured to amend the stored page in response to the amended data and control signals.

24. (Previously presented) The non volatile memory of claim 23, wherein:

the column parity circuit further comprises, for each column parity:

an exclusive-or logic circuit configured to receive bits from the associated half of the columns and generate a result of an exclusive-or operation on bits from the associated half of the columns; and

a parity accumulator including:

a flip flop having an input and an output; and

an exclusive-or gate having a first input coupled to the output of the flip flop, a second input to receive the result of the exclusive-or operation on the bits from the associated half of the columns, and an output coupled to the input of the flip flop;

the line parity circuit further comprises:

an exclusive-or logic circuit configured to generate a result of an exclusive-or operation on bits from a selected one of the lines;

for each line parity, a parity accumulator including:

a flip flop having an input and an output;

an exclusive-or gate having a first input coupled to the output of the flip flop, a second input, and an output coupled to the input of the flip flop; and

a gate having a first input configured to receive an associated clock control signal, a second input coupled to the output of the exclusive-or logic circuit, and an output coupled to the second input of the exclusive-or gate; and

the page buffer further comprises:

a buffering and sensing logic block coupled to the data storage field and including a plurality of bitlines;

a plurality of unit blocks, each unit block including:

an input/output line;

a plurality of latches, each latch coupled to an associated bitline of the buffering and sensing logic block; and

a plurality of column gates coupled to the latches and configured to selectively couple one of the latches to the input/output line in response to a plurality of column gating signals;

wherein the input/output lines of the unit blocks are coupled to the error correction circuit.

25. (Previously presented) The non volatile memory of claim 24, further comprising:

control signal generator coupled to the first inputs of the gates and the column gates, the clock control signal generator configured to generate the clock control signals associated with the gates and the column gating signals;

wherein the control signal generator is configured to generate the clock control signals associated with gates associated with a line indicated by the column gating signals.

26. (Previously presented) The nonvolatile memory of claim 1, wherein the page buffer includes only one register.